

# BIPOLAR ANALOG INTEGRATED CIRCUIT

# $\mu$ PC2708TB

### 5 V, SUPER MINIMOLD SILICON MMIC MEDIUM OUTPUT POWER AMPLIFIER

#### DESCRIPTION

The  $\mu$ PC2708TB is a silicon monolithic integrated circuit designed as buffer amplifier for BS/CS tuners. This IC is packaged in super minimold package which is smaller than conventional minimold.

The  $\mu$ PC2708TB has compatible pin connections and performance to  $\mu$ PC2708T of conventional minimold version. So, in the case of reducing your system size,  $\mu$ PC2708TB is suitable to replace from  $\mu$ PC2708T.

This IC is manufactured using NEC's 20 GHz fr NESAT™ III silicon bipolar process. This process uses silicon nitride passivation film and gold electrodes. These materials can protect chip surface from external pollution and prevent corrosion/migration. Thus, this IC has excellent performance, uniformity and reliability.

#### FEATURES

- High-density surface mounting : 6-pin super minimold package (2.0 × 1.25 × 0.9 mm)
- Wideband response :  $f_u = 2.9$  GHz TYP. @ 3 dB bandwidth
- Medium output power :  $P_{O(sat)} = +10$  dBm TYP. @  $f = 1$  GHz with external inductor
- Supply voltage :  $V_{CC} = 4.5$  to 5.5 V
- Power gain :  $G_P = 15$  dB TYP. @  $f = 1$  GHz
- Port impedance : input/output 50  $\Omega$

#### APPLICATIONS

- 1st IF amplifiers in BS/CS converters, etc.
- 1st IF stage buffer in BS/CS tuners, etc.

#### ORDERING INFORMATION

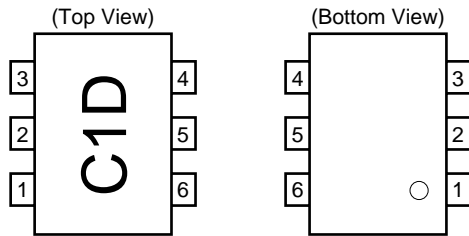
Part Number	Package	Marking	Supplying Form
$\mu$ PC2708TB-E3	6-pin super minimold	C1D	Embossed tape 8 mm wide. 1, 2, 3 pins face the perforation side of the tape. Qty 3 kpcs/reel.

**Remark** To order evaluation samples, please contact your local NEC sales office (Part number for sample order:  $\mu$ PC2708TB).

**Caution** Electro-static sensitive devices

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.  
Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

**PIN CONNECTIONS**



Pin No.	Pin Name
1	INPUT
2	GND
3	GND
4	OUTPUT
5	GND
6	V <sub>CC</sub>

**PRODUCT LINE-UP OF 5 V-BIAS SILICON MMIC MEDIUM OUTPUT POWER AMPLIFIER**

(T<sub>A</sub> = +25°C, V<sub>CC</sub> = V<sub>out</sub> = 5.0 V, Z<sub>s</sub> = Z<sub>L</sub> = 50 Ω)

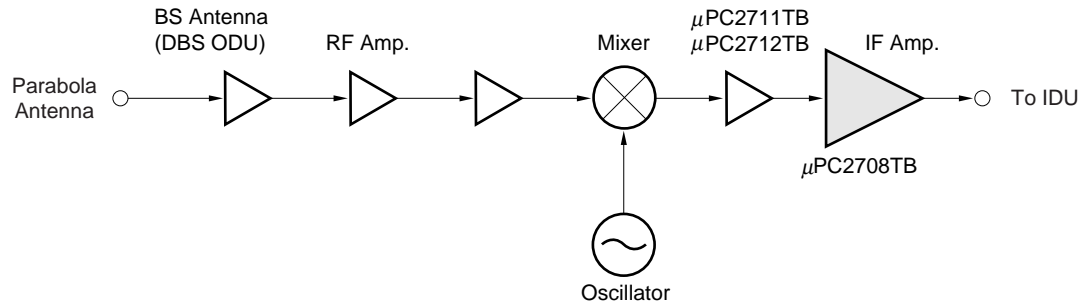
Part No.	f <sub>u</sub> (GHz)	P <sub>O(sat)</sub> (dBm)	G <sub>P</sub> (dB)	NF (dB)	I <sub>cc</sub> (mA)	Package	Marking
$\mu$ PC2708T	2.9	+10.0	15	6.5 @f = 1 GHz	26	6-pin minimold	C1D
$\mu$ PC2708TB						6-pin super minimold	
$\mu$ PC2709T	2.3	+11.5	23	5 @f = 1 GHz	25	6-pin minimold	C1E
$\mu$ PC2709TB						6-pin super minimold	
$\mu$ PC2710T	1.0	+13.5	33	3.5 @f = 0.5 GHz	22	6-pin minimold	C1F
$\mu$ PC2710TB						6-pin super minimold	
$\mu$ PC2776T	2.7	+8.5	23	6.0 @f = 1 GHz	25	6-pin minimold	C2L
$\mu$ PC2776TB						6-pin super minimold	

**Remark** Typical performance. Please refer to **ELECTRICAL CHARACTERISTICS** in detail.

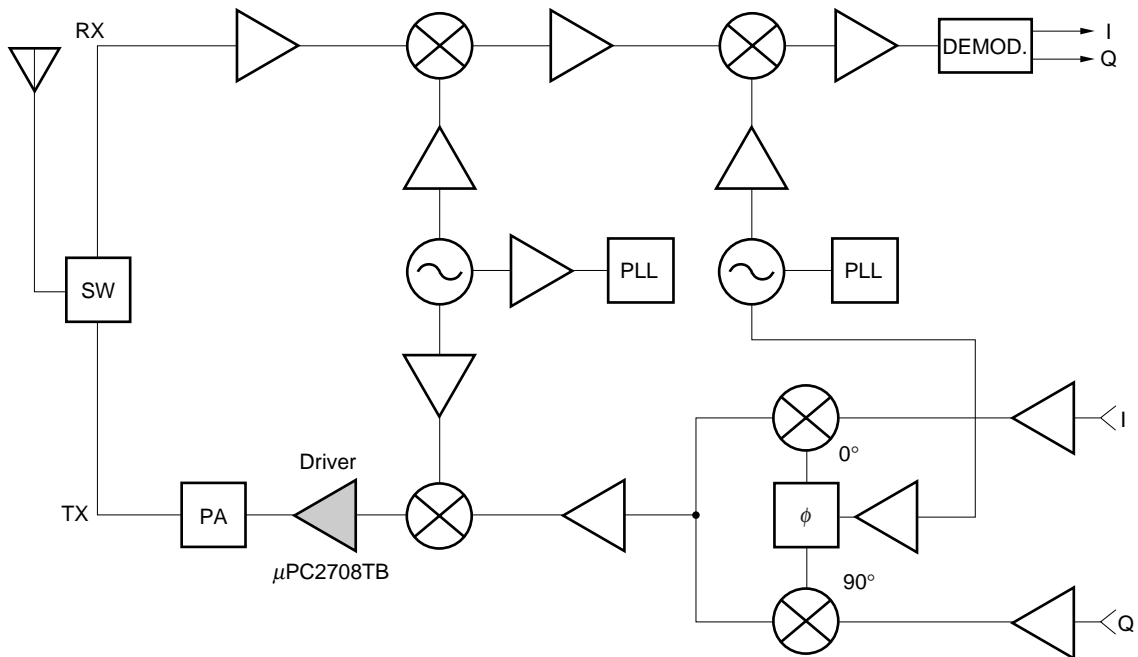
**Caution** The package size distinguishes between minimold and super minimold.

SYSTEM APPLICATION EXAMPLE

EXAMPLE OF DBS CONVERTERS



EXAMPLE OF 2.4 GHz BAND RECIEVER



**PIN EXPLANATION**

Pin No.	Pin Name	Applied Voltage (V)	Pin Voltage (V) <small>Note</small>	Function and Applications	Internal Equivalent Circuit
1	INPUT	–	1.16	Signal input pin. A internal matching circuit, configured with resistors, enables 50 Ω connection over a wide band. A multi-feedback circuit is designed to cancel the deviations of $h_{FE}$ and resistance. This pin must be coupled to signal source with capacitor for DC cut.	
4	OUTPUT	Voltage as same as $V_{CC}$ through external inductor	–	Signal output pin. The inductor must be attached between $V_{CC}$ and output pins to supply current to the internal output transistors.	
6	$V_{CC}$	4.5 to 5.5	–	Power supply pin, which biases the internal input transistor. This pin should be externally equipped with bypass capacitor to minimize its impedance.	
2 3 5	GND	0	–	Ground pin. This pin should be connected to system ground with minimum inductance. Ground pattern on the board should be formed as wide as possible. All the ground pins must be connected together with wide ground pattern to decrease impedance difference.	

**Note** Pin voltage is measured at  $V_{CC} = 5.0\text{ V}$

**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Conditions	Ratings	Unit
Supply Voltage	V <sub>CC</sub>	T <sub>A</sub> = +25°C, Pin 4 and 6	6	V
Total Circuit Current	I <sub>CC</sub>	T <sub>A</sub> = +25°C	60	mA
Power Dissipation	P <sub>D</sub>	Mounted on doublesided copper clad 50 × 50 × 1.6 mm epoxy glass PWB (T <sub>A</sub> = +85°C)	270	mW
Operating Ambient Temperature	T <sub>A</sub>		-40 to +85	°C
Storage Temperature	T <sub>stg</sub>		-55 to +150	°C
Input Power	P <sub>in</sub>	T <sub>A</sub> = +25°C	+10	dBm

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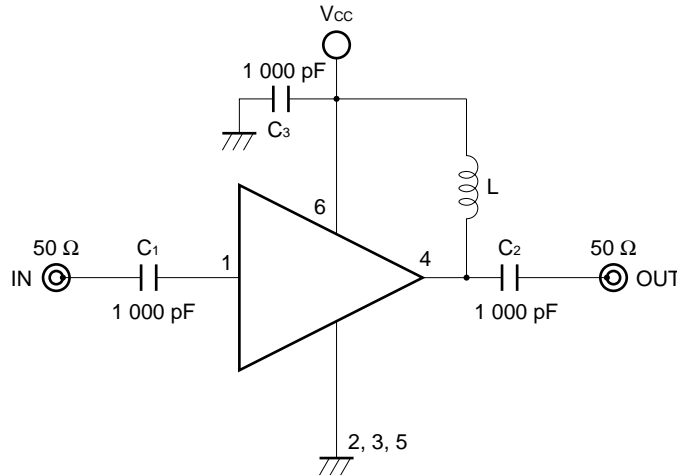
**RECOMMENDED OPERATING RANGE**

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Remark
Supply Voltage	V <sub>CC</sub>	4.5	5.0	5.5	V	The same voltage should be applied to pin 4 and 6.
Operating Ambient Temperature	T <sub>A</sub>	-40	+25	+85	°C	

**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = +25°C, V<sub>CC</sub> = V<sub>out</sub> = 5.0 V, Z<sub>s</sub> = Z<sub>L</sub> = 50 Ω)**

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Circuit Current	I <sub>CC</sub>	No input Signal	20	26	33	mA
Power Gain	G <sub>P</sub>	f = 1 GHz	13.0	15.0	18.5	dB
Saturated Output Power	P <sub>O(sat)</sub>	f = 1 GHz, P <sub>in</sub> = 0 dBm	+7.5	+10.0	-	dBm
Noise Figure	NF	f = 1 GHz	-	6.5	8.0	dB
Upper Limit Operating Frequency	f <sub>u</sub>	3 dB down below flat gain at f = 0.1 GHz	2.7	2.9	-	GHz
Isolation	ISL	f = 1 GHz	18	23	-	dB
Input Return Loss	RL <sub>in</sub>	f = 1 GHz	8	11	-	dB
Output Return Loss	RL <sub>out</sub>	f = 1 GHz	16	20	-	dB
Gain Flatness	ΔG <sub>P</sub>	f = 0.1 to 2.6 GHz	-	±0.8	-	dB

TEST CIRCUIT



COMPONENTS OF TEST CIRCUIT FOR MEASURING ELECTRICAL CHARACTERISTICS

	Type	Value
C <sub>1</sub> , C <sub>2</sub>	Bias Tee	1 000 pF
C <sub>3</sub>	Capacitor	1 000 pF
L	Bias Tee	1 000 nH

EXAMPLE OF ACTUAL APPLICATION COMPONENTS

	Type	Value	Operating Frequency
C <sub>1</sub> to C <sub>3</sub>	Chip Capacitor	1 000 pF	100 MHz or higher
L	Chip Inductor	300 nH	10 MHz or higher
		100 nH	100 MHz or higher
		10 nH	1.0 GHz or higher

INDUCTOR FOR THE OUTPUT PIN

The internal output transistor of this IC consumes 20 mA, to output medium power. To supply current for output transistor, connect an inductor between the Vcc pin (pin 6) and output pin (pin 4). Select large value inductance, as listed above.

The inductor has both DC and AC effects. In terms of DC, the inductor biases the output transistor with minimum voltage drop to output enable high level. In terms of AC, the inductor make output-port impedance higher to get enough gain. In this case, large inductance and Q is suitable.

CAPACITORS FOR THE Vcc, INPUT AND OUTPUT PINS

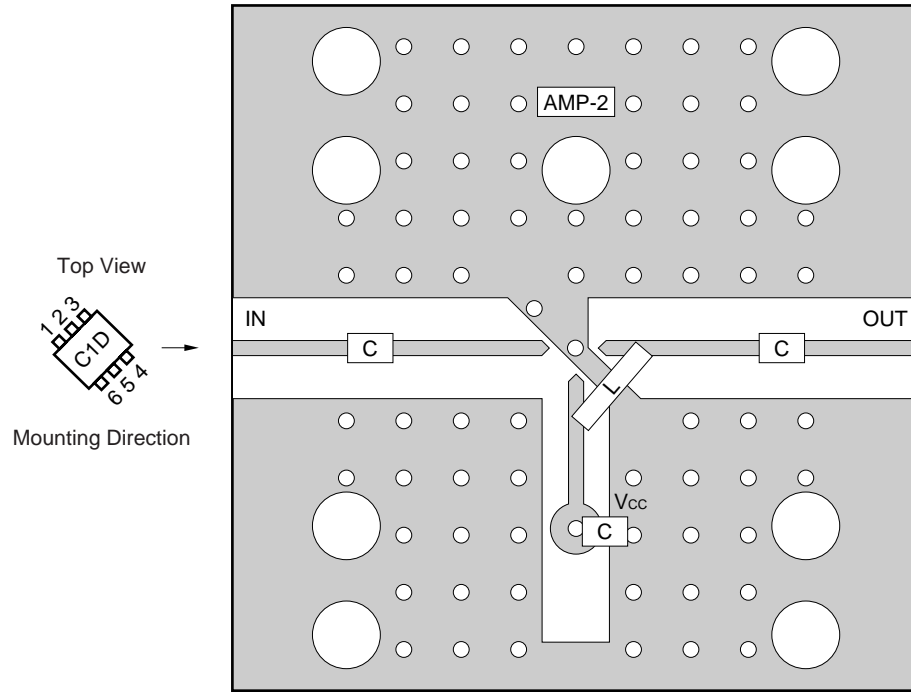
Capacitors of 1000 pF are recommendable as the bypass capacitor for the Vcc pin and the coupling capacitors for the input and output pins.

The bypass capacitor connected to the Vcc pin is used to minimize ground impedance of Vcc pin. So, stable bias can be supplied against Vcc fluctuation.

The coupling capacitors, connected to the input and output pins, are used to cut the DC and minimize RF serial impedance. Their capacitance are therefore selected as lower impedance against a 50 Ω load. The capacitors thus perform as high pass filters, suppressing low frequencies to DC.

To obtain a flat gain from 100 MHz upwards, 1000 pF capacitors are used in the test circuit. In the case of under 10 MHz operation, increase the value of coupling capacitor such as 10000 pF. Because the coupling capacitors are determined by equation,  $C = 1/(2 \pi Rf_c)$ .

ILLUSTRATION OF THE TEST CIRCUIT ASSEMBLED ON EVALUATION BOARD



COMPONENT LIST

	Value
C	1 000 pF
L	300 nH

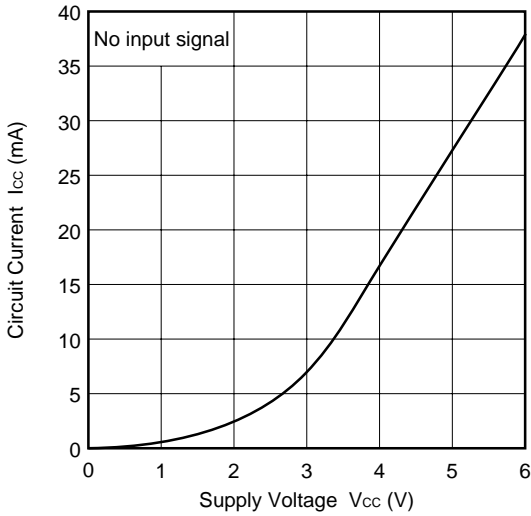
Notes

1. 30 × 30 × 0.4 mm double sided copper clad polyimide board.
2. Back side: GND pattern
3. Solder plated on pattern
4. ○ ○ : Through holes

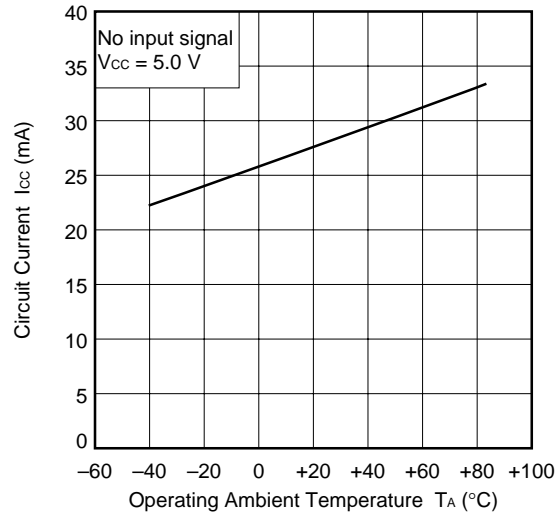
For more information on the use of this IC, refer to the following application note: **USAGE AND APPLICATION OF SILICON MEDIUM-POWER HIGH-FREQUENCY AMPLIFIER MMIC (P12152E)**.

TYPICAL CHARACTERISTICS (Unless otherwise specified,  $T_A = +25^\circ\text{C}$ )

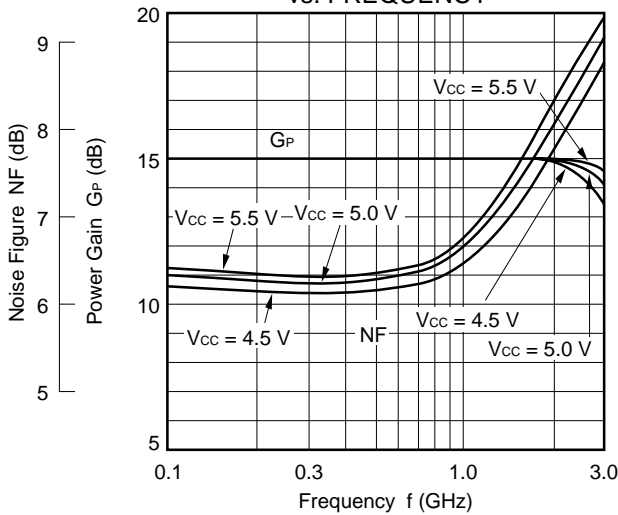
CIRCUIT CURRENT vs. SUPPLY VOLTAGE



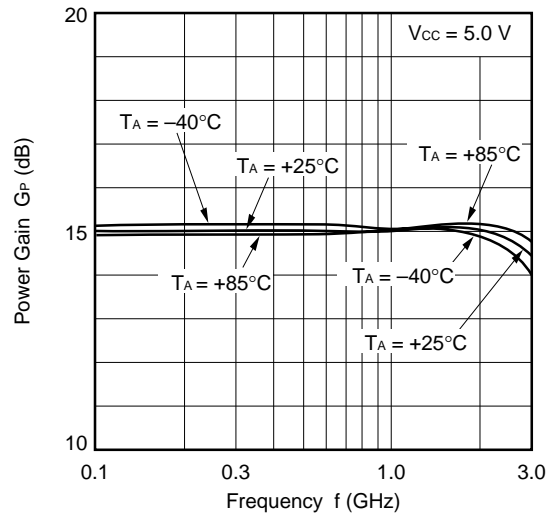
CIRCUIT CURRENT vs. OPERATING AMBIENT TEMPERATURE



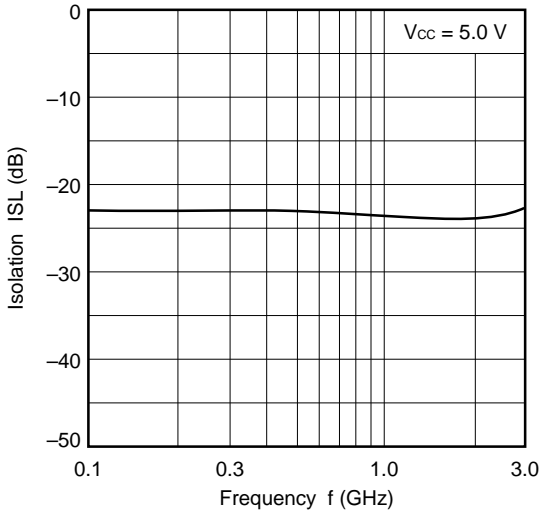
NOISE FIGURE, POWER GAIN vs. FREQUENCY



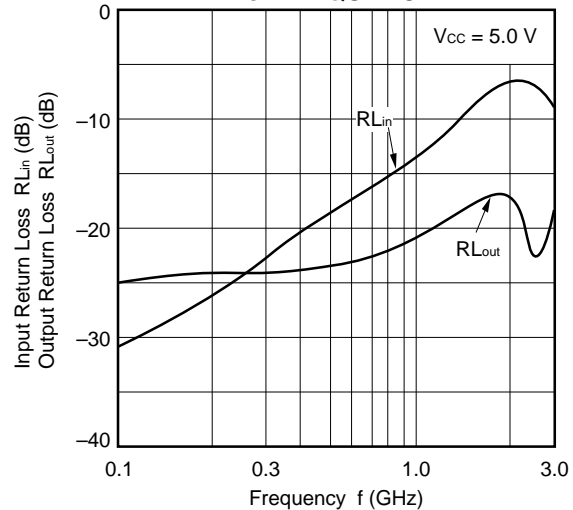
POWER GAIN vs. FREQUENCY



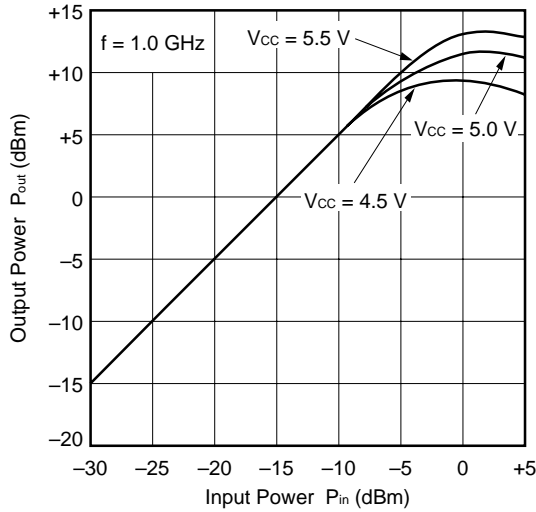
ISOLATION vs. FREQUENCY



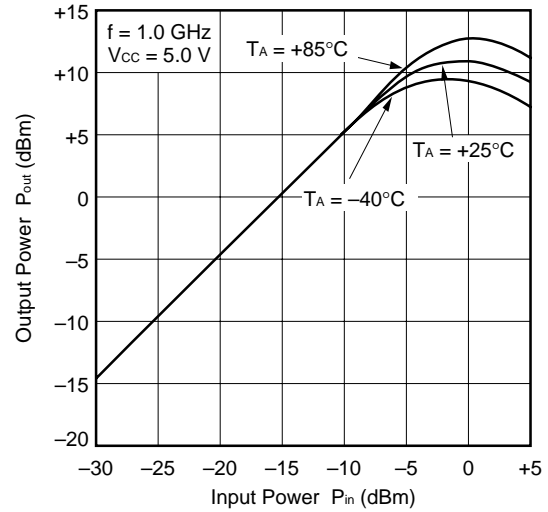
INPUT RETURN LOSS, OUTPUT RETURN LOSS vs. FREQUENCY



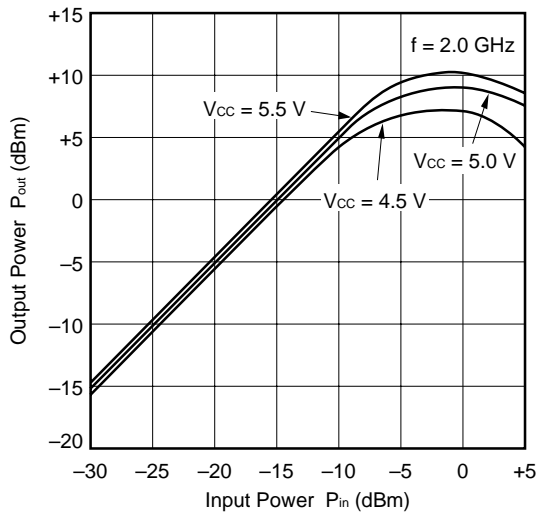
OUTPUT POWER vs. INPUT POWER



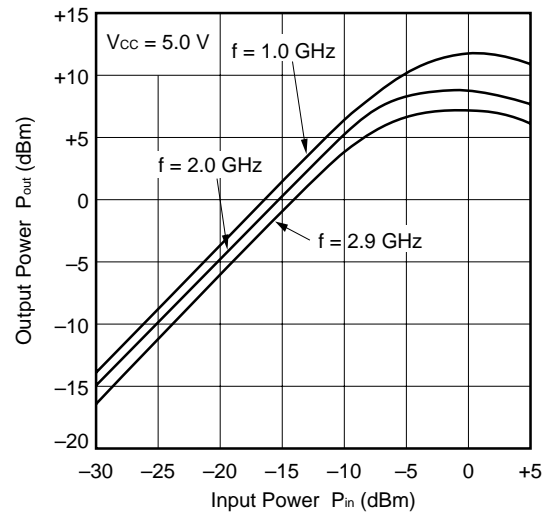
OUTPUT POWER vs. INPUT POWER



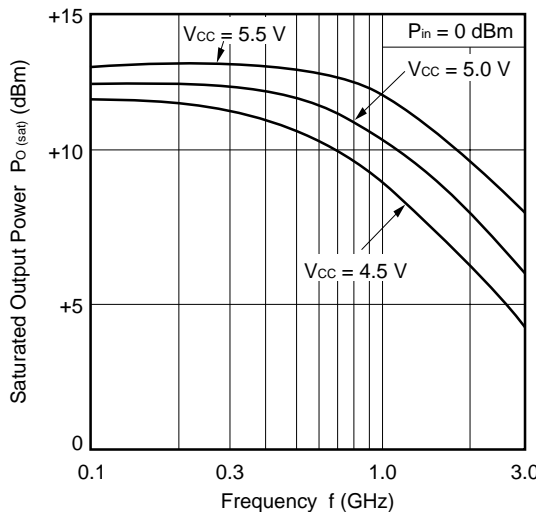
OUTPUT POWER vs. INPUT POWER



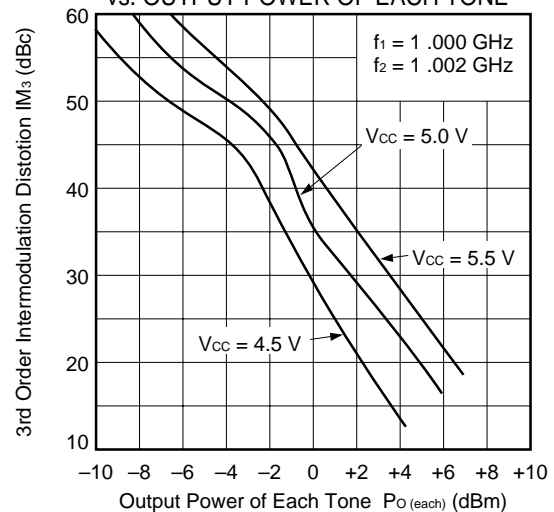
OUTPUT POWER vs. INPUT POWER



SATURATED OUTPUT POWER vs. FREQUENCY



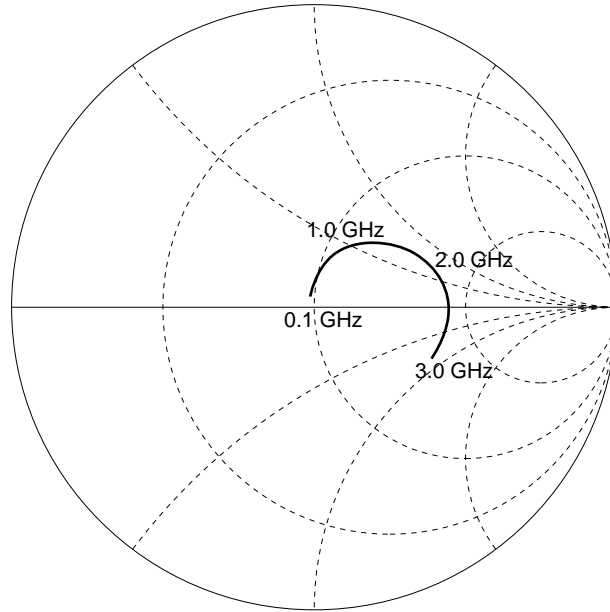
3RD ORDER INTERMODULATION DISTORTION vs. OUTPUT POWER OF EACH TONE



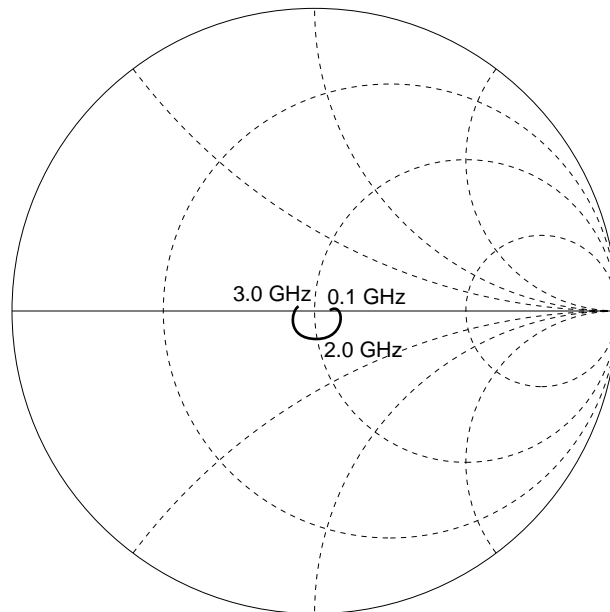
**Remark** The graphs indicate nominal characteristics.

S-PARAMETERS ( $T_A = +25^\circ\text{C}$ ,  $V_{CC} = V_{out} = 5.0\text{ V}$ )

S<sub>11</sub>-FREQUENCY



S<sub>22</sub>-FREQUENCY



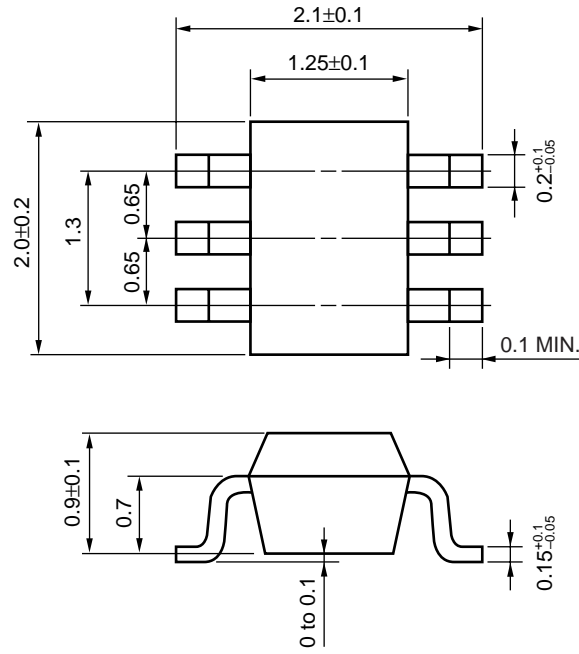
TYPICAL S-PARAMETER VALUES (T<sub>A</sub> = +25°C)

V<sub>CC</sub> = V<sub>out</sub> = 5.0 V, I<sub>CC</sub> = 27 mA

FREQUENCY MHz	S <sub>11</sub>		S <sub>21</sub>		S <sub>12</sub>		S <sub>22</sub>		K
	MAG.	ANG.	MAG.	ANG.	MAG.	ANG.	MAG.	ANG.	
100.0000	0.039	138.9	5.815	-4.8	0.077	-0.8	0.051	0.9	1.34
200.0000	0.053	119.7	5.822	-9.8	0.075	-1.5	0.048	1.4	1.36
300.0000	0.069	106.7	5.815	-14.3	0.074	-0.6	0.049	5.9	1.38
400.0000	0.088	97.2	5.813	-18.8	0.074	-0.5	0.054	8.9	1.36
500.0000	0.105	91.6	5.794	-23.8	0.072	-1.1	0.054	8.8	1.39
600.0000	0.123	84.9	5.823	-28.4	0.071	-0.6	0.056	10.4	1.40
700.0000	0.144	79.7	5.871	-33.0	0.070	0.1	0.060	11.5	1.40
800.0000	0.164	74.7	5.890	-38.2	0.071	0.5	0.065	11.6	1.37
900.0000	0.186	70.7	5.938	-42.8	0.073	2.3	0.072	11.1	1.34
1000.0000	0.205	66.1	5.960	-47.6	0.070	1.0	0.074	8.2	1.36
1100.0000	0.226	61.7	6.072	-52.7	0.069	3.3	0.075	9.4	1.34
1200.0000	0.245	57.7	6.097	-57.5	0.070	4.4	0.082	5.6	1.31
1300.0000	0.263	53.7	6.174	-63.0	0.067	2.5	0.085	0.6	1.33
1400.0000	0.286	48.6	6.275	-68.4	0.069	5.0	0.091	-4.6	1.28
1500.0000	0.308	44.3	6.371	-74.3	0.070	5.4	0.092	-8.2	1.24
1600.0000	0.328	40.7	6.419	-79.8	0.066	7.1	0.097	-12.6	1.26
1700.0000	0.344	36.2	6.470	-85.9	0.067	5.6	0.096	-19.6	1.23
1800.0000	0.364	31.0	6.555	-92.1	0.069	8.2	0.100	-23.9	1.18
1900.0000	0.382	26.0	6.542	-98.3	0.070	8.4	0.100	-32.0	1.15
2000.0000	0.395	21.2	6.570	-104.7	0.070	8.7	0.101	-38.9	1.13
2100.0000	0.405	16.8	6.528	-111.3	0.070	10.1	0.100	-47.2	1.12
2200.0000	0.417	11.8	6.527	-118.5	0.071	9.4	0.096	-57.2	1.09
2300.0000	0.427	6.6	6.438	-124.7	0.072	9.5	0.098	-66.1	1.09
2400.0000	0.431	2.2	6.336	-131.3	0.071	10.7	0.095	-76.5	1.09
2500.0000	0.431	-3.0	6.247	-138.1	0.072	12.8	0.098	-86.1	1.09
2600.0000	0.434	-8.2	6.127	-145.0	0.071	15.4	0.094	-99.9	1.10
2700.0000	0.423	-12.3	5.952	-151.7	0.071	14.5	0.088	-116.7	1.14
2800.0000	0.419	-17.1	5.816	-158.2	0.070	16.1	0.081	-134.4	1.18
2900.0000	0.408	-21.5	5.619	-165.0	0.073	15.3	0.074	-149.7	1.19
3000.0000	0.400	-26.2	5.354	-171.5	0.074	17.1	0.065	-170.3	1.24
3100.0000	0.386	-29.3	5.134	-177.4	0.075	17.1	0.053	172.8	1.28

★ PACKAGE DIMENSIONS

6-PIN SUPER MINIMOLD (UNIT: mm)



**NOTES ON CORRECT USE**

- (1) Observe precautions for handling because of electro-static sensitive devices.
- (2) Form a ground pattern as wide as possible to minimize ground impedance (to prevent undesired oscillation).  
All the ground pins must be connected together with wide ground pattern to decrease impedance difference.
- (3) The bypass capacitor should be attached to Vcc line.
- (4) The inductor must be attached between Vcc and output pins. The inductance value should be determined in accordance with desired frequency.
- (5) The DC cut capacitor must be attached to input and output pin.

**RECOMMENDED SOLDERING CONDITIONS**

This product should be soldered under the following recommended conditions. For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared Reflow	Package peak temperature: 235°C or below Time: 30 seconds or less (at 210°C) Count: 3, Exposure limit: None <sup>Note</sup>	IR35-00-3
VPS	Package peak temperature: 215°C or below Time: 40 seconds or less (at 200°C) Count: 3, Exposure limit: None <sup>Note</sup>	VP15-00-3
Wave Soldering	Soldering bath temperature: 260°C or below Time: 10 seconds or less Count: 1, Exposure limit: None <sup>Note</sup>	WS60-00-1
Partial Heating	Pin temperature: 300°C Time: 3 seconds or less (per side of device) Exposure limit: None <sup>Note</sup>	—

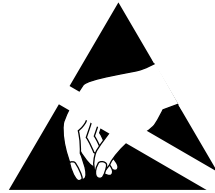
**Note** After opening the dry pack, keep it in a place below 25°C and 65% RH for the allowable storage period.

**Caution** Do not use different soldering methods together (except for partial heating).

For details of recommended soldering conditions for surface mounting, refer to information document **SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL (C10535E)**.

[MEMO]

[MEMO]



# ATTENTION

OBSERVE PRECAUTIONS  
FOR HANDLING  
ELECTROSTATIC  
SENSITIVE  
DEVICES

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